Listing of Claims

Claims 1-2 (Canceled).

3. (Currently amended) ~~The method of Claim 2, wherein said step of forming a silicon carbide drift layer is preceded by the steps of:~~ A method of forming a silicon carbide MOSFET device having a 10kV or higher blocking voltage rating, comprising the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique or a high-temperature CVD growth technique; **[[and]]**

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute some fraction of silicon atoms to phosphorus atoms within the silicon carbide boule;

forming a silicon carbide wafer from the irradiated silicon carbide boule;

forming a boule-grown silicon carbide drift layer having a net n-type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3} by annealing the silicon carbide wafer at a sufficient temperature to reduce a trap density therein;

forming a p-type silicon carbide base region on the silicon carbide drift layer;

forming an n-type silicon carbide source region that defines a p-n rectifying junction with the p-type silicon carbide base region; and

forming a gate electrode on the p-type silicon carbide base region.

4. (Currently amended) The method of Claim 3 **[[1]]**, wherein the silicon carbide drift layer has a thickness in a range from between about 100 μm and about 400 μm.

Claims 5-7 (Canceled).

8. (Currently amended) ~~The method of Claim 6, wherein said step of forming a silicon carbide drift layer is preceded by the steps of:~~ A method of forming a high-voltage silicon carbide device, comprising the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique or a high-temperature CVD growth technique; **[[**and**]]**

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute some fraction of silicon atoms to phosphorus atoms within the silicon carbide boule;

forming a silicon carbide wafer from the irradiated silicon carbide boule;

forming a boule-grown silicon carbide drift layer having a net n-type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3} by annealing the silicon carbide wafer at a sufficient temperature to achieve a characteristic minority carrier lifetime in excess of 50 nanoseconds therein; and

forming n-type and p-type silicon carbide layers on the silicon carbide drift layer.

9. (Currently amended) The method of Claim 8 **[[**5**]]**, wherein the silicon carbide drift layer has a thickness in a range from between about 100 μm and about 400 μm.

Claims 10-32 (Canceled).

33. (Currently amended) ~~The method of Claim 32,~~ A method of forming a silicon carbide JFET having a 10kV or higher blocking voltage rating, comprising the steps of:

forming a boule-grown silicon carbide drift layer having a net n-type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3};

forming an n-type silicon carbide epilayer on the silicon carbide drift layer;

forming an n-type silicon carbide source region in the n-type silicon carbide epilayer; and

forming a p-type silicon carbide gate electrode on the n-type silicon carbide epilayer;

wherein said step of forming an n-type silicon carbide epilayer is preceded by the step of forming a p-type silicon carbide buried region in the silicon carbide drift layer;

wherein said step of forming an n-type silicon carbide epilayer comprises forming an n-type silicon carbide epilayer that defines a p-n rectifying junction with the p-type silicon carbide buried region and a non-rectifying junction with the silicon carbide drift layer; and

wherein said step of forming a p-type silicon carbide gate electrode comprises forming a p-type silicon carbide gate electrode that extends opposite a portion of the p-type silicon carbide buried region.

34. (Original) The method of Claim 33, further comprising the step of forming a source electrode that ohmically contacts the n-type silicon carbide source region and the p-type silicon carbide buried region.

35. (Currently amended) The method of Claim 33 **[[32]]**, wherein said step of forming a boule-grown silicon carbide drift layer comprises annealing a boule-grown silicon carbide wafer at a sufficiently high temperature to reduce a density of traps therein.

36. (Currently amended) ~~The method of Claim 32, wherein said step of forming a silicon carbide drift layer is preceded by the steps of:~~ A method of forming a silicon carbide JFET having a 10kV or higher blocking voltage rating, comprising the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique; **[[and]]**

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute silicon atoms to phosphorus atoms within the silicon carbide boule;

forming a silicon carbide drift layer having a net n-type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3} from the irradiated silicon carbide boule;

forming an n-type silicon carbide epilayer on the silicon carbide drift layer;

forming an n-type silicon carbide source region in the n-type silicon carbide epilayer; and

forming a p-type silicon carbide gate electrode on the n-type silicon carbide epilayer.

37. (Currently amended) The method of Claim 36 **[[32]]**, wherein the silicon carbide drift layer has a thickness in a range from between about 100 μm and about 400 μm.

Claim 38-40 (Canceled).

41. (Currently amended) ~~The method of Claim 38, wherein said step of forming a silicon carbide drift layer is preceded by the steps of:~~ A method of forming a silicon carbide MOSFET device having a 10kV or higher blocking voltage rating, comprising the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique; **[[and]]**

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute some fraction of silicon atoms to phosphorus atoms within the silicon carbide boule;

forming a silicon carbide drift layer having a net first conductivity type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3} from the irradiated silicon carbide boule;

forming a second conductivity type silicon carbide base region on the silicon carbide drift layer;

forming a first conductivity type silicon carbide source region that defines a p-n rectifying junction with the second conductivity type silicon carbide base region; and

forming a gate electrode on the second conductivity type silicon carbide base region.

42. (Currently amended) The method of Claim 41 [[38]], wherein the silicon carbide drift layer has a thickness in a range from between about 100 μm and about 400 μm.

Claims 43-45 (Canceled).

46. (New) A method of forming a high-voltage silicon carbide device, comprising the steps of:

forming a silicon carbide boule using a seeded sublimation growth technique or a high-temperature CVD growth technique;

irradiating the silicon carbide boule with thermal neutrons of sufficient fluence to thereby transmute some fraction of silicon atoms to phosphorus atoms within the silicon carbide boule;

forming a silicon carbide wafer from the irradiated silicon carbide boule; and

forming a boule-grown silicon carbide drift layer having a net n-type dopant concentration therein that is less than about $2x10^{15}$ cm^{-3} by annealing the silicon carbide wafer at a sufficient temperature to achieve a characteristic minority carrier lifetime in excess of 50 nanoseconds therein.

47. (New) The method of Claim 46, wherein the silicon carbide wafer layer has a thickness in a range from between about 100 μm and about 400 μm.